What is claimed is:

1. A system for canceling interference caused by propagation of a transmit signal transmitted from a transmit antenna to a receive antenna, the system comprising:

an interference cancellation signal generator that generates a time-delayed and amplitude-reduced representation of said transmit signal; and

a summing stage, operably coupled to said interference cancellation signal generator and said receive antenna, that subtracts said time-delayed and amplitude-reduced representation of said transmit signal from a receive signal received at said receive antenna to substantially cancel said interference;

wherein said interference cancellation signal generator comprises a programmable optical delay line that introduces a variable amount of optical delay to an optical signal derived from said transmit signal.

2. A system according to claim 1, wherein:

the resultant signal produced by said summing stage is supplied to a receiver for subsequent processing.

3. A system according to claim 1, wherein:

said programmable optical delay line comprises a plurality of programmable delay sections providing different resolution optical delays.

4. A system according to claim 1, wherein:

said programmable optical delay line comprises a substrate upon which is integrated a network of polymer-based passive waveguides and optical switching nodes.

5. A system according to claim 4, wherein:

said optical switching nodes comprise optical amplifiers that compensate for losses and a directional coupler.

6. A system according to claim 5, wherein:

said directional coupler is realized from an inversion quantum-well channel device structure.

7. A system according to claim 1, wherein:

said programmable optical delay line comprises an optoelectronic circuit that includes a network of on-chip passive waveguides and directional couplers.

8. A system according to claim 7, wherein:

said direction couplers are realized from an inversion quantum-well channel device structure.

9. A system according to claim 1, wherein:

said programmable optical delay line comprises an integrated circuit that includes a length of passive waveguide that is heated by resistive heaters integral thereto.

10. A system according to claim 1, wherein:

said programmable optical delay line comprises a fixed length optical waveguide.

11. A system according to claim 1, further comprising:

first means for converting samples of said transmit signal in electrical form into a digital optical signal.

12. A system according to claim 11, wherein:

said first means comprises a sigma-delta modulator.

13. A system according to claim 12, wherein:

said sigma delta modulator includes an integration stage comprising a first heterojunction thyristor device providing high gain amplification.

14. A system according to claim 12, wherein:

said sigma delta modulator includes a second heterojunction thyristor device adapted to contemporaneously perform 1-bit analog-to-digital conversion and electrical-to-optical conversion of the result of the 1-bit analog-to-digital conversion.

15. A system according to claim 14, further comprising:

a current source and a third heterojunction thyristor device that operate in response to a sampling clock signal supplied thereto to reset said second heterojunction thyristor when a sampling period defined by said sampling clock signal has ended.

16. A system according to claim 15, wherein:

said sampling clock signal comprises one of an electrical clock signal and optical clock signal.

17. A system according to claim 14, further comprising:

another heterojunction thyristor adapted to operated as a 1-bit DAC in accordance with an output signal produced by said second heterojunction thyristor.

18. A system according to claim 17, wherein:

said output signal comprises one of an electrical signal and optical signal representing results of said 1-bit analog-to-digital conversion performed by said first heterojunction thyristor.

19. A system according to claim 12, wherein:

all of said electronic and optoelectronic circuit elements that realize said sigma-delta modulator are formed from a common inversion quantum-well channel device structure.

20. A system according to claim 11, further comprising:

second means for converting a digital optical signal supplied thereto into a corresponding analog signal in the electrical domain.

21. A system according to claim 20, wherein:

said second means comprises a series of elements including a heterojunction thyristor adapted to operate as a photoreceiver and a low-pass filter/integrator stage.

22. A programmable optical delay line comprising:

a plurality of programmable delay sections integral to a substrate, said sections providing different resolution optical delays.

23. A programmable optical delay line according to claim 22, wherein:

one of said sections comprises a network of polymer-based passive waveguides and optical switching nodes.

24. A programmable optical delay line according to claim 23, wherein:

said optical switching nodes comprise optical amplifiers that compensate for losses and a directional coupler.

25. A programmable optical delay line according to claim 24, wherein:

said directional coupler is realized from an inversion quantum-well channel device structure.

26. A programmable optical delay line according to claim 22, wherein:

one of said sections comprise an optoelectronic circuit that includes a network of on-chip passive waveguides and directional couplers.

27. A programmable optical delay line according to claim 26, wherein:

said directional couplers are realized from an inversion quantum-well channel device structure.

28. A programmable optical delay line according to claim 22, wherein:

one of said sections comprise an integrated circuit that includes a length of passive waveguide that is heated by resistive heaters integral thereto.

29. An integrated circuit comprising:

a network of on-chip passive waveguides and two-channel directional couplers, said two-channel directional couplers realized from an inversion quantum-well channel device structure.

30. An integrated circuit according to claim 29, wherein:

optical signals are selectively switched between said channels utilizing evanescent coupling.

31. An integrated circuit according to claim 30, wherein:

optical signals are selectively switched between channels of a given directional coupler based upon voltage levels applied to gate and source terminals for said given directional coupler.

32. An integrated circuit according to claim 31, wherein:

said channels of a given directional coupler are separated by a narrow passive region formed via impurity free vacancy disordering.

33. A sigma-delta-type analog-to-digital converter comprising:

at least one of

an integration stage comprising a resistor, a first heterojunction thyristor device providing high gain amplification, and a feedback capacitor; and

a second heterojunction thyristor device adapted to contemporaneously perform 1-bit analog-to-digital conversion and electrical-to-optical conversion of the result of the 1-bit analog-to-digital conversion.

34. A sigma-delta-type analog-to-digital converter according to claim 33, wherein:

said first heterojunction thyristor device includes a injector terminal electrically coupled to a quantum well channel, a bias current source operably coupled to said injector terminal to provide a desired switching voltage having high gain characteristics, and bias resistance that sets a bias current through said first heterojunction device at a point corresponding to said desired switching voltage.

35. A sigma-delta-type analog-to-digital converter according to claim 33, further comprising:

a current source and a third heterojunction transistor that operate in response to a sampling clock signal supplied thereto to reset said second heterojunction thyristor when a sampling period defined by said sampling clock signal has ended.

36. A sigma-delta-type analog-to-digital converter according to claim 35, wherein:

said sampling clock signal comprises one of an electrical clock signal and optical clock signal.

37. A sigma-delta-type analog-to-digital converter according to claim 33, further comprising:

another heterojunction thyristor adapted to operated as a 1-bit DAC in accordance with an output signal produced by said second heterojunction thyristor.

38. A sigma-delta-type analog-to-digital converter according to claim 37, wherein:

said output signal comprises one of an electrical signal and optical signal representing results of said 1-bit analog-to-digital conversion performed by said second heterojunction thyristor.

39. A sigma-delta-type analog-to-digital converter according to claim 33, further comprising:

a decimation circuit operably coupled to electrical output of said second heterojunction thyristor device.

40. A sigma-delta-type analog-to-digital converter according to claim 33, wherein:

all of said electronic and optoelectronic circuit elements that realize said sigma-delta converter are formed from a common inversion quantum-well channel device structure.